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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,069	12/15/2003	Seong-Min Choe	51876P440	5251

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,069	CHOE, SEONG-MIN	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12-14 and 17* is/are rejected.

7)☒ Claim(s) *15, 16, 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

Claims 1, 8, 12, 14, and 17 are objected to because of the following informalities:

Claim 1, lines 4-5, "a first and a second inner resistor" appears to be "a first and a second inner resistors".

Claim 8, line 1, "of one" should be deleted.

Claim 12, line 4, "a first and a second inner resistor" appears to be "a first and a second inner resistors"; and on line 5 "the first and the second inner resistor" appears to be "the first inner resistor".

Claim 14, line 4, "a reference voltage" appears to be "the reference voltage".

Claim 17, line 4, "the first and the second inner resistors" appears to be "the first inner resistor"; and on lines 6-8, "third resistor" appears to be "third inner resistor".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12 and 17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The recitation, "the first and the second inner resistors used to generate a push-up code" in claim 12 and 17 was not found

either in specification or drawings. Rather, only the first inner resistor is used to generate a push-up code and the second and the third inner resistors are used to generate a push-down code (see pp. 7-10 of specification and 201, 210, and 211 in Fig. 1).

For the purposes of expediting prosecution on the merits of the claims, the examiner has attempted to construe the claims to the extent possible for the following art rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12-14 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 6,429,679 B1, Kim hereinafter).

Regarding claim 12, Kim discloses, in Fig. 20, an on-DRAM termination resistance control method for adjusting resistance within a semiconductor memory device (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)) that performs an on-DRAM termination operation, comprising the steps of:

(a) adjusting resistances of a first and a second inner resistor (3, 4) based on an external reference resistor (RQ), the first inner resistor used to generate a push-up code (see "To UP Driver");

(b) adjusting a resistance of a third inner resistor (8) based on the second inner resistor (via 6, 165, 166, 167 and the lines that connects to 8) that is adjusted at the step (a), the third inner resistor used to generate a pull-down code (see "To LOW Driver"); and

(c) controlling the steps (a) and (b) for a predetermined commanded adjustment time (col. 7, lines 65+).

Regarding claim 13, Kim discloses, in Fig. 20, that wherein the step (a) includes the steps of:

(d) comparing (by 161) the voltage between both ends of the external reference resistor coupled to the first inner resistor with a reference voltage (Vref); and

(e) adjusting the resistances of the first and the second inner resistors depending on the comparison result (output of 161) of the step (d) (see the lines from 163 to 3 and 240 to 4).

Regarding claim 14, Kim discloses, in Fig. 20, that wherein the step (b) includes steps of:

(f) comparing (by 165) the voltage between both ends of the third inner resistor coupled to the second inner resistor with a reference voltage (Vref); and

(g) adjusting the resistance of the third inner resistor depending on the comparison result (output of 165) of the step (f) (see the line connecting from 167 to 8).

Regarding claim 17, Kim discloses, in Fig. 20, an on-DRAM termination resistance control circuit for use in a semiconductor memory device (it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987)) that performs an On-DRAM termination operation, comprising:

a push-up resistance adjusting means (161, 163) for adjusting resistances of a first (3) and a second (4) inner resistors based on an external reference resistor (RQ), the first inner resistor used to generate a push-up code (see "To UP Driver");

a pull-down resistance adjusting means (165, 167) for adjusting a resistance of a third inner resistor (8) based on the second inner resistor that is adjusted by the push-up resistance adjusting means, the third inner resistor used to generate a pull-down code; and

a resistance adjustment control means (164, 168) for controlling the operations of the push-up resistance adjusting means and the pull-down resistance adjusting means for the predetermined adjustment time (col. 7, lines 65+).

Allowable Subject Matter

Claims 1-11 are allowable over the prior art.

Claims 15, 16, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Kim, taken alone or in combination of other references, does not teach or fairly suggest a method or an on-DRAM termination resistance control circuit comprising, among other things, that wherein the resistance adjustment control means includes a ring oscillator controlling means for outputting a control signal to start an operation and finish the operation for the predetermined commanded adjustment time depending on an external resistance adjust command (claim 1); outputting a pulse at every cycle while oscillating based on

the control signal (claim 15); and that wherein the push-up code and the pull-down code are respectively input to a push-up decoder and a pull-down decoder in an interface circuit for performing an on-DRAM termination operation (claim 18), as set forth in the claims.

Response to Arguments

Applicant's arguments filed May 4, 2006 have been fully considered but they are not persuasive.

Applicant argues, on page 11, that "Applicant's claimed invention asserts both first and second inner resistors 201 and 210 are used to generate a push-up code; a third inner resistor is used to generate a pull-down code". However, after carefully reviewing the specification and the drawing, only the first inner resistor 201 is used to generate a push-up code PU and the second and the third inner resistors 210 and 211 are used to generate a push-down code, PD (see pp. 7-10 of specification and 201, 210, and 211 in Fig. 1). Therefore, the examiner has attempted to construe the claims to the extent possible for the art rejection as discussed above in order to expediting prosecution on the merits of the claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Art Unit 2819

dc

DANIEL CHANG
PRIMARY EXAMINER